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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/419,523
Filing Date: October 18, 1999
Appellant(s): PETERSEN, PAUL

Robert A. Manware
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 8, 2006 appealing from the Office action mailed May 30, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

A first Appeal Brief was filed in this application to the Board of Patent Appeals and Interferences on April 9, 2003. The Board of Patent Appeals and Interferences mailed a decision to affirm the rejections of all claims on August 31, 2004, in Appeal No. 2004-0037.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner herewith.

(A) Claims 41-51, 53-60, 62-65 and 67 were rejected for failing to comply with the enablement requirement of 35 U.S.C. § 112, first paragraph.

(B) Claims 41-51, 53-60, 62-65 and 67 were rejected for failing to comply with the written description requirement of 35 U.S.C. § 112, first paragraph.

GROUNDS OF REJECTION NOT ON REVIEW

The following grounds of rejection have not been withdrawn by the examiner, but they are not under review on appeal because they have not been presented for review in the appellant's brief.

(A) Claims 43 and 56-57 are rejected as being unpatentable over Arai (U.S. Patent No. 5,280,599) in view of Yoshizawa (U.S. Patent No. 5,787,464), further in view of Helm et al. (U.S. Patent No. 5,129,069).

(B) Claims 44 is rejected as being unpatentable over Arai (U.S. Patent No. 5,280,599) in view of Yoshizawa (U.S. Patent No. 5,787,464), further in view of Cowell (U.S. Patent No. 5,860,134).

(C) Claims 46, 47 and 50 is rejected as being unpatentable over Arai (U.S. Patent No. 5,280,599) in view of Yoshizawa (U.S. Patent No. 5,787,464), further in view of Dresser et al. (U.S. Patent No. 5,446,860).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Ware, Frederick, "Direct RMC.d1 Data Sheet", RAMBUS, DL0036-00.7 (Aug 7-13, 1998), pp. 1-104.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 41-42, 45, 48-49, 51, 53-55, 58-60, 62-65, and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai (U.S. Patent No. 5,280,599), in view of Yoshizawa et al (U.S. Patent No. 5,787,464). In addition, Ware (RAMBUS "Direct RMC.d1 Data Sheet", DL0036-00.7, hereinafter "RAMBUS") is cited as extrinsic evidence.

With respect to claims 41-42, 45, 48-49, 51, 53-55, 58-60, 62-65, and 67, the definition of "memory configuration information," provided in appellant's disclosure is "type, amount, and operating characteristics of memory" (note page 5 of appellant's specification and Figure 3 of appellant's drawings). The claimed "upgrade options" and "memory characteristics" have been given their broadest reasonable interpretation.

With regard to claims 41, 54 and 62, Arai determines a maximum (expanded) capacity of memory address space not necessarily in the context of memory devices per se and does so up to 8 megabytes. Note the showings in Figures 1 and 2 as well as Figure 9. The discussion at the bottom of column 1 of Arai relates to the prior art EMS system where the discussion beginning at line 31 clearly indicates that there exists prior art software or instructions on which to control the so-called EMM (Expanded Memory Manager), whereas the bottom of column 1 beginning at line 54 indicates that the memory address space was known to be one megabyte or more. Figures 1 and 2 collectively show that up to 8 megabytes as well may be separately addressable; such feature is shown as well in Figure 9. Thus the maximum storage capacity or the residual memory

capacity appears to be 8 megabytes. These teachings and showings confirm that Arai teaches the feature of the last clause of claims 41, 54 and 62 of "determining memory upgrade options based on the determined memory capacity of the computer system."

In addition, these capabilities are expanded upon based upon the Figure 3 showing and its discussion beginning at column 3 where the BIOS ROM 13 has programs resident in it which perform an operation represented by the flow chart shown in Figure 5 which determines the nature of the maximum expansion/extension of the memory according to Arai's contributions in the art. Thus, there are clearly additional teachings of software or instructions relating to programmable devices (see the explicit recitations of these capabilities in independent claims 12, 18, 32 and 38). Column 4 continues this discussion of the software orientation as well as makes clear that the system of Arai relates to memory capacity determinations in various configuration embodiments, as well as the feature that it is the software that controls these determinations as claimed.

Note the discussion of Figure 9 at column 6 of Arai as well. In accordance with the showing in Figure 4, it is the user who is given the option to determine the nature of the expansion/extension of the memory because the display unit 17 of Figure 3 displays the options, a portion of which appears to be depicted as box 18 in Figure 4.

However, Arai alone has no explicit teaching of relating these expansion abilities to memory devices per se.

Nonetheless, Yoshizawa makes explicit what has been implied by Arai's teachings alone. Yoshizawa makes clear that it is known in the art to use various expansion slots on which *memory* may be added or replaced.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Yoshizawa's teachings of allowing the insertion and extraction of memory modules in the computer system of Arai, since even Yoshizawa's title reveals the memory expansion capability, which clearly dovetails with the memory expansion abilities of Arai, since it is in the context of extraction and insertion. Various embodiments are shown in Yoshizawa but, as the examiner has made reference, the showings in Figures 1 through 3A are sufficient for illustrative purposes here. The logic shown in Figure 3A permits the user of the system to extract and insert (replace) and/or the ability to just insert/add memory in a single or a plurality of memory slots within a computer system. The showing in Figure 8 relates more specifically to a replacement operation and the showing in Figure 11 relates to the determination of open slots from which memory may be expanded or added. Also dovetailing with Arai's teachings noted earlier with respect to capacity determinations, these logic flow charts in Figures 3A, 8 and 11 show that a determination is made of the capacity of the system once extraction/insertion operations or replacing operations have occurred. As revealed in the last sentence of the abstract, "Memory may be expanded in computer systems that do not have an open memory slot by replacing the installed memory with a memory device having a larger capacity." All of these contributions of Yoshizawa are in addition to what

has been recognized at column 1 of the prior art of the ability to expand memory by adding more memory in existing, extra memory slots as well as adding or expanding memory using memory elements in single slot computers where the new memory elements have larger capacity. In either case, it is clear from the summary of the invention that memory may be replaced to the extent recited in independent claims 21, 32 and 38.

Thus, the features noted in Yoshizawa are compelling reasons to modify and/or embellish upon the generalized teachings in Arai. The feature of Yoshizawa's teachings of allowing the insertion and extraction of memory modules while the computer system is online or otherwise operating is an additional basis for the desirable combinability to the artisan of Yoshizawa with Arai.

As for "executing a software routine to determine a maximum number of memory devices that can be supported *per memory bus channel* of the computer system," this was a well known technique used to determine total memory capacity in prior art computer systems and was "readily understood by one of ordinary skill in the art", as conceded by appellant on page 10 of the Appeal Brief. RAMBUS is cited as extrinsic evidence of such, as disclosed on the top of page 40 of RAMBUS, wherein address values were programmed into configuration fields to determine total device size. Page 41 discloses configuration. Page 42 discloses initialization (software routine) that determines present devices. Page 40 discloses that a device field has been programmed at 5-bits, therefore allowing a maximum of 32 devices per stick. Pages 56-58

further disclose configuration and RDRAM initialization. Also, see page 73, which discloses the algorithm InitDev. The system must determine whether it is actually there or not (a characteristic other than size). Whether it is present or not will affect the capacity. This is discussed in RAMBUS on page 1, which discloses the optional 1 to 32 RDRAMS that may be connected to the controller, page 40, which discusses the configuration options (number of regions, e.g.), page 41, which discusses the addressing options based on the configuration, page 42, which discloses that initialization "automatically" (i.e., using a configuration routine including instructions to obtain memory configuration information) manages the configuration, including whether a device is present or not, page 45, which elaborates on the mapping techniques, page 57, which shows the actual configuration commands for the number of devices present, and pages 72-75, which discuss initialization of the devices, including "serial presence detect."

With respect to claims 42, 55, 63, and 65, the act of obtaining memory configuration information comprising obtaining an indication of an installed system memory amount is disclosed by Arai as explained above and in column 2, lines 46-60, for example.

With respect to claims 45 and 58, the act of obtaining memory configuration information comprising accessing a non-volatile storage device is disclosed by Arai in figure 3 as ROM/BIOS, and further discussed in column 3, lines 53-59.

With respect to claims 48-49, 59, and 64, obtaining the maximum number of memory devices and maximum amount of memory for the computer system are inherent, as the number of address bits, according to the binary number system upon which computers operate, indicate the "amount of memory" which includes the number of "devices." Note also the citations provided above for the rejections of claims 41, 54 and 62.

With respect to claim 51, providing memory upgrade options to a user is disclosed in column 6, line 45, which discusses a "window" for such information. Note also Figure 4.

With respect to claims 53, 60, and 67, the characteristic comprising a limit on the number of memory devices that can be installed on a memory channel regardless of the number of open slots is inherent. Note the RAMBUS reference discussed above – only so much space may be addressed by the number of address bits being used in the entire system, even if one memory slot has a 1 gigabit memory, but the other slots are all open, if that is the maximum memory addressable by the address bus, then that is the only memory that will work in the system. Furthermore, no system can support unlimited or infinite memory.

(10) Response to Argument

With respect to appellant's arguments "A" and "B", these are moot in view of the withdrawal of all rejections under 35 U.S.C. 112, first paragraph.

With respect to appellant's argument "C", it is noted that the patentability of most of the features of appealed claims 41-42, 45, 48-49, 51, 53-55, 58-60, 62-65, and 67 has already been decided by the Board of Patent Appeals and Interferences in the decision mailed on August 31, 2004.

As for the limitation "automatically" (note, e.g., claim 41), this limitation has already been considered because it means using "a configuration routine including instructions to obtain memory configuration information", which was in claim 38, which fell with the affirmation of the rejections on August 31, 2004.

Some of the appealed claims are simply combinations of prior claims that which the Board of Patent Appeals and Interferences has already considered. For example, appealed claim 54 is a combination of the features of previous claim 32 and claim 30. Note that both of these claims fell with the affirmation of the rejections on August 31, 2004.

In fact, a side-by-side comparison of previously appealed claims 1-40 with presently appealed claims 41-42, 45, 48-49, 51, 53-55, 58-60, 62-65, and 67 shows that the presently appealed claims are merely a combination of the previous independent claims with various previous dependent claims – *all of which fell with the affirmation of the rejections on August 31, 2004.*

There is only one exception: claims 41 and 62 include the limitation "executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system". This limitation was not presented in claims 1-40 and thus was not decided by the Board of Patent Appeals and Interferences.

Applicant's arguments directed to all other features or limitations of the claims are moot, since the patentability of such has already been decided by the Board of Patent Appeals and Interferences (*res judicata*).

As for "executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system", the Board of Patent Appeals and Interferences explicitly stated that Arai used software to determine memory capacity (note page 5 of the decision of August 31, 2004).

Thus, there is only one issue remaining – was it well known to determine a memory capacity based on a maximum number of memory devices that can be supported *per memory bus channel* of the computer system? Appellant's seem to think so. In fact, in an attempt to overcome the previous rejections under 35 U.S.C. 112, first paragraph, appellant explicitly admitted that using this technique to determine total memory capacity in prior art computer systems and was "readily understood by one of ordinary skill in the art". Note page 10 of the Appeal Brief. In making the point, appellant relies on the prior knowledge that there is a limit of 32 devices per memory channel, and this information may be stored in a non-volatile memory device. Thus, appellant has described exactly

what occurs in the RAMBUS system (note page 40), which was cited as extrinsic evidence that such a technique was well known. Furthermore, in the paragraph spanning pages 5 and 6 of appellant's specification, appellant has already admitted that this feature of the RAMBUS in particular was well known to those of ordinary skill in the art of computer system memory design.

Consequently, appellant's efforts to argue against the applicability of the RAMBUS reference on page 12 of the Appeal Brief are in stark contradiction to the arguments that were presented on page 10 of the same document.

(11) Related Proceeding(s) Appendix

Copies of the court or Board decision(s) identified in the Related Appeals and Interferences section of this examiner's answer are provided herein.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

B. James Peikari

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